said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in op ration, an electronic signal stored in said latch is retained for at least one clock cycle.

5. (once amended) The circuit of claim 4, wherein said differential sense circuit comprises:

a first inverter and a second inverter, said first and second inverters each having an input terminal and an output terminal, said input terminal of said first and second inverter being coupled respectively to a pull-down terminal, said output terminal of said first and second inverters being coupled respectively to a pull-up terminal, said output terminal of said first and second inverter being respectively coupled to opposite terminals of said latch, said input terminal of said first and second inverter being respectively coupled to a non-inverted output terminal and an inverted output terminal of said p-type sense amp;

a third inverter having an input terminal and an output terminal, said input terminal being coupled to said inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to said first inverter; and

a fourth inverter having an input terminal and an output terminal, said input terminal being coupled to said non-inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to said second inverter.

17. (twice amended) An integrated circuit (IC) comprising:

a plurality of datapaths, at least one of said datapaths comprising:

a differential circuit and a differential sense latch, wherein said differential sense latch comprises a differential sense circuit and a jam-latch coupled, such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam latch.